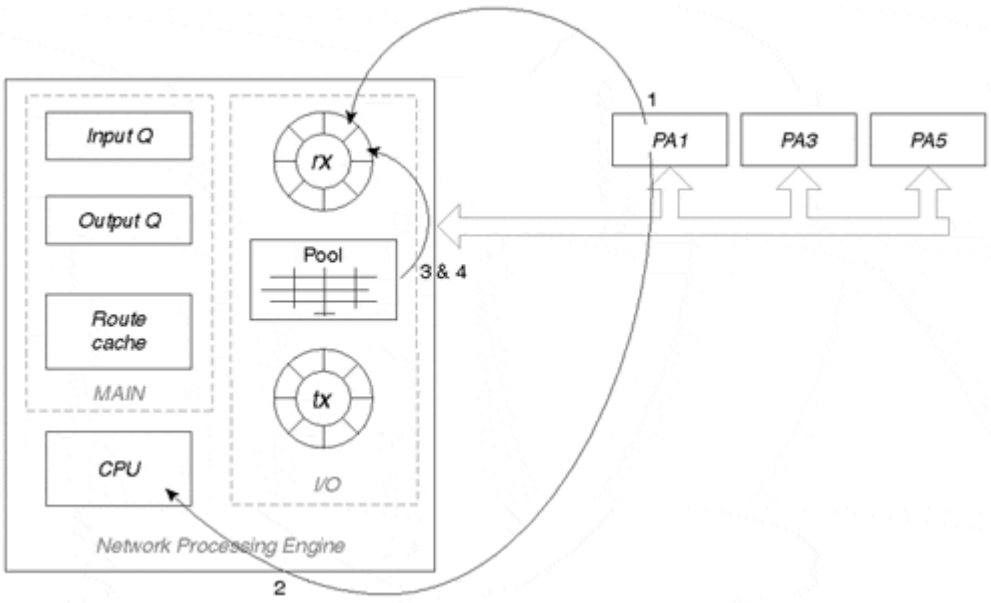
Packet Switching on the Cisco 7200 Series Routers

The Cisco 7200 supports process switching, fast switching, and Cisco Express Forwarding (CEF), but doesn't support any form of distributed switching. The main CPU in the NPE performs all the switching tasks.

Packet Receive Stage

Figure 5-6 illustrates what occurs when a packet is received.

Figure 5-6. Receiving a Packet



Step 1. The packet is copied from the media into a series of particles linked to the interface's receive ring. The particles can reside in either I/O memory or PCI memory depending on the platform and the interface's media speed.

Step 2. The interface raises a receive interrupt to the CPU.

Step 3. The IOS acknowledges the interrupt and begins attempting to allocate particles to replace the ones filled on the interface's receive ring. IOS checks the interface's private pool first, and then checks the public normal pool if none are in the private pool. If not enough particles exist to replenish the receive ring, the packet is dropped (the packet's particles on the receive ring are flushed) and the *no buffer* counter is incremented.

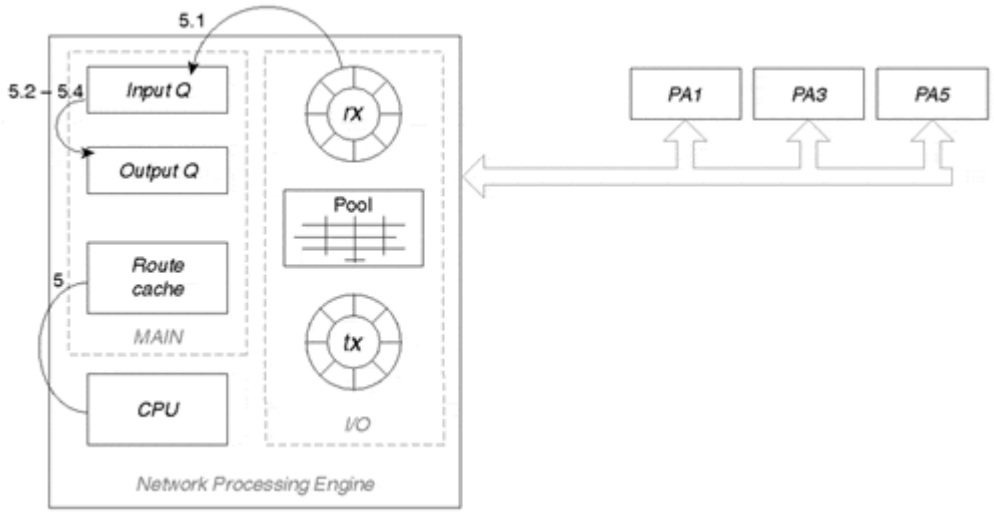
IOS also throttles the interface in this case. When an interface is throttled on the 7200, all received packets are ignored until the interface is unthrottled. IOS unthrottles the interface after the depleted particle pool is replenished with free particles.

Step 4. IOS links the packet's particles in the receive ring together, and then links them to a particle buffer header. It then replenishes the receive ring with the newly allocated particles by linking them to the ring in place of the packet's particles.

Packet Switching Stage

Now that the packet is in particles, IOS switches the packet. Figure 5-7 illustrates the process as described in the sequential list following the figure.

Figure 5-7. Switching a Packet



Step 5. The switching code first checks the route cache (fast or CEF) to see if it can fast switch the packet. If the packet can be switched during the interrupt, it skips to Step 6; otherwise, it continues to prepare the packet for process switching.

Step 5.1. The packet is coalesced into a contiguous buffer (system buffer). If no free system buffer exists to accept the packet, it's dropped and the **no buffer** counter is incremented, as indicated in the output of the **show interface** command:

```
Router#show interface
Ethernet2/1 is up, line protocol is up
….
  Output queue 0/40, 0 drops; input queue 0/75, 0 drops
  5 minute input rate 5000 bits/sec, 11 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
     1903171 packets input, 114715570 bytes, 1 no buffer
     Received 1901319 broadcasts, 0 runts, 0 giants, 1 throttles
….
```

If IOS can't allocate a system buffer to coalesce a particle buffer, it also throttles the interface and increments the **throttles** counter, as indicated in the preceding **show interface** command output example. All input traffic is ignored while an interface is throttled. The interface remains throttled until IOS has free system buffers available for the interface.

Step 5.2. When the packet is coalesced, it is queued for process switching and the process that handles this type of packet is scheduled to run. The receive interrupt then is dismissed.

Step 5.3. Let's assume this is an IP packet. When the IP Input process runs, it consults the routing table and discovers the outbound interface. It consults the tables associated with the outbound interface and locates the MAC header that needs to be placed on the packet (not shown in Figure 5-7).

Step 5.4. After the packet has been switched successfully, it's copied into the output queue for the outbound interface.

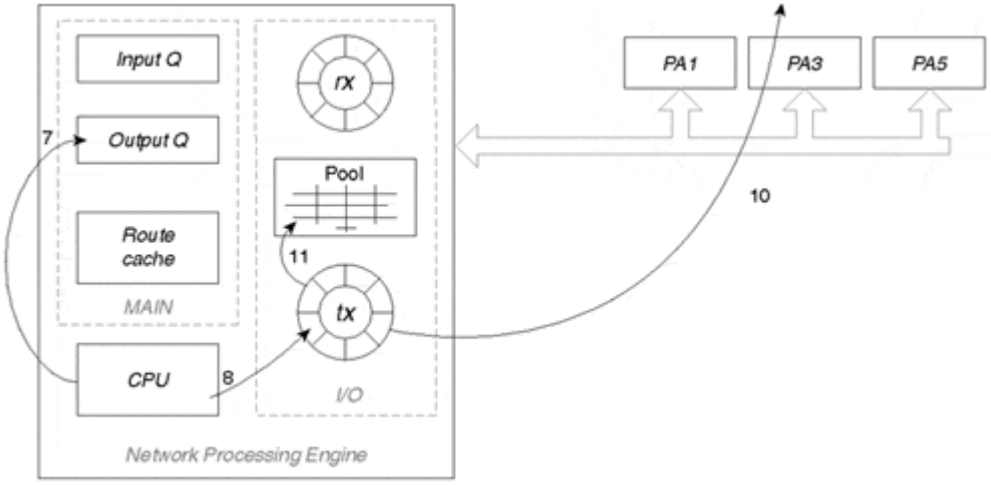
Step 5.5. From here, IOS proceeds to the transmit stage.

Step 6. The IOS switching code (fast or CEF) rewrites the MAC header in the packet for its destination (not shown in Figure 5-7). If the new MAC header is larger than the original header, IOS allocates a new particle from the F/S pool and inserts it at the beginning of the chain of particles to hold the larger header.

Packet Transmit Stage

Now you have a successfully switched packet, with its MAC header rewritten. Figure 5-8 picks up the story.

Figure 5-8. Transmitting the Packet



The packet transmit stage operates differently depending on whether IOS is fast switching the packet (fast or CEF) or process switching the packet. The following sections cover the packet transmit stage in the fast and process switching environments for Cisco 7200 series routers.

Packet Transmit Stage: Fast Switching and CEF

The following list describes the packet transmit stage in a fast switching environment:

Step 7. IOS first checks the interface's output queue. If the output queue is not empty or the interface's transmit ring is full, IOS queues the packet on the output queue and dismisses the receive interrupt. The packet eventually gets transmitted either when another process-switched packet arrives or when the interface issues a transmit interrupt. If the output queue is empty and the transmit ring has room, IOS continues to Step 8.

Step 8. IOS links each of the packet's particles to the interface's transmit ring and dismisses the receive interrupt.

Step 9. The interface media controller polls its transmit ring and detects a new packet to be transmitted.

Step 10. The interface media controller copies the packet from its transmit ring to the media and raises a transmit interrupt to the CPU.

Step 11. The IOS acknowledges the transmit interrupt and frees all the transmitted packet's particles from the transmit ring, returning them to their originating particle pool.

Step 12. If any packets are waiting on the interface's output queue (presumably because the transmit ring was full up until now), IOS removes the packets from the queue and links their particles or contiguous buffers to the transmit ring for the media controller to see (not shown in Figure 5-8).

Step 13. IOS dismisses the transmit interrupt.

Packet Transmit Stage: Process Switching

The following list describes the packet transmit stage in a process switching environment. Figure 5-8 does not illustrate these steps.

Step 14. IOS checks the size of the next packet on the output queue and compares it to the space left on the interface's transmit ring. If enough space exists on the transmit ring, IOS removes the packet from the output queue and links its contiguous buffer (or particles) to the transmit ring. Note, if multiple packets exist on the output queue, IOS attempts to drain the queue, putting all the packets on the interface's transmit ring.

Step 15. The interface's media controller polls its transmit ring and detects a new packet to be transmitted.

Step 16. The interface media controller copies the packet from its transmit ring to the media and raises a transmit interrupt to the CPU.

Step 17. The IOS acknowledges the transmit interrupt and frees the transmitted packet's contiguous buffer (or particles) from the transmit ring, returning them to their originating pool.

Last updated on 12/5/2001

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